ABSTRACT OF THE DISCLOSURE

A semiconductor memory device operating in synchronization with an external clock signal, includes memory cells arrayed in two dimension, word lines and bit lines connected to the memory cells, IO lines connected to the bit lines, and a sense amplifier connected to the IO lines and activated by a sense amplifier enable signal. After the word line is selected, an internal clock signal is generated by delaying the rising and falling edges of the external clock signal input to the memory device. A timing at which the internal clock signal changes from a first state to a second state is delayed by a predetermined time to make the sense amplifier enable signal active, and a timing at which the internal clock signal changes from the second state to the first state is delayed by a shorter period than the predetermined time to make the sense amplifier enable signal inactive.